REMARKS

Claims 1-22 are pending in the application.

Claims 1-22 have been rejected.

Claims 21-22 have been amended as set forth herein.

Claims 1-22 remain pending in this application.

Reconsideration of the claims is respectfully requested.

I. CLAIM REJECTIONS -- 35 U.S.C. § 112

Claims 2 and 14-20 were rejected under 35 U.S.C. § 112, first paragraph as claiming subject matter that is not described in the specification in a manner enabling one skilled in the relevant art to make or use the claimed invention. This rejection is respectfully traversed.

Any analysis of whether a particular claim is supported by the disclosure in an application requires a determination of whether that disclosure, when filed, contained sufficient information regarding the subject matter of the claims as to enable one skilled in the pertinent art to make and use the claimed invention. MPEP § 2164.01, p. 2100-193 (8th ed., rev. 4, October 2005). The test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation. *Id.* A patent need not teach, and preferably omits, what is well known in the art. *Id.* The Patent Office has the initial burden of establishing a reasonable basis to question the enablement provided for the claimed invention. MPEP § 2164.04 at 2100-197. The minimal requirement for a proper enablement rejection is to give reasons for the uncertainty of the enablement. *Id.*

In regard to Claims 2 and 15, the Office Action objects to the limitation "each hash table is allocated a *smallest number of memory blocks sufficient* to hold prefixes for which no collision occurs within the respective table." The specification, paragraph [0027], describes an "optimization to minimize collisions ... in use of block-based SRAM allocation for each hash table," wherein a small block is first allocated and, when rehashing no longer yields an empty slot, another block is allocated. Further, Claims 2 and 15, as originally filed recite "at least one hash table is contained within a smallest number of memory blocks sufficient to hold all required prefixes for which no collision occurs within the at least one hash table." Therefore, the specification (including the claims) as filed inherently contains a written description of the limitation.

In regard to Claim 14, the Office Action objects to the limitation "each hash table is allocated a different group of memory blocks from a plurality of memory blocks." The specification, starting at paragraph [0024], discloses dividing memory into small blocks that are dynamically allocated such that the hash table size can be tailored. Therefore, the specification as filed contains a written description of the limitation.

Claims 21 and 22 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter. The Applicants have amended Claim21 and 22 as shown above. The Applicants note that Claim 22 was previously mis-numbered as Claim 21. However, the Examiner has correctly determined the proper numbering of the claim as Claim 22 in the § 112 rejection. Accordingly, the Applicants herein have renumbered the claim as Claim 22.

Accordingly, the Applicants respectfully request that the Examiner withdraw the § 112 rejection of Claims 2 and 14-22.

II. CLAIM REJECTIONS -- 35 U.S.C. § 102

Claims 1, 5-14 and 18-20 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,665,297 to *Hariguchi, et al* (hereinafter "Hariguchi"). This rejection is respectfully traversed.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131, p. 2100-76 (8th ed., rev. 4, October 2005) (*citing In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990)). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. *Id.* (*citing Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987)).

Independent Claims 1 and 10 claim each recite that each hast table is allocated a group of the memory blocks based on a size of the respective hash table. Similarly, independent Claim 14 recites that a number of memory blocks allocated to a hash table is based on a size of the respective hash table.

The Office Action argues that *Hariguchi* (column 6, line 66-column 7, line 2 and column 8, line 56-column 9, line 7) teaches this feature of independent Claims 1, 10 and 14. The Office Action states "hash bucket 160 comprises memory blocks for storing route entries; the size of the route

entries in the hash bucket of the hash table is 'a size of the hash table'." (Office Action, dated June 26, 2008, page 4). The cited portions of *Hariguchi* is copied below:

> In the hash bucket stage 94, a hash bucket 160 stores network addresses and output pointers at addresses corresponding to the hash value of their associated masked destination addresses. During a second pipeline clock cycle, (Hariguchi, Col 6, ln. 66 – Col. 7, ln. 2).
>
> During operation, the routing table 40 (FIG. 2) is updated. New route entries are added to the hash buckets and to the CAM and existing route entries are deleted from the hash buckets and CAM.
>
> Referring back to both FIGS. 4 and 5, the addition of a new route entry to the hash bucket 160 of the routing table 40 will be described. For an add operation, on pipeline clock cycle 1, a destination address is supplied by the microprocessor as the CPU_addr and is input to the mask circuit 154 in response to the Search/CPU command line. The hash function generator circuit 156 generates a hash value based on the supplied address. The microprocessor also outputs data corresponding to the output pointer associated with the destination address to the data mask circuit 168. The data mask circuit 168 acts as a driver when writing data to the hash bucket to allow the data from the CPU to be stored into the hash bucket. If the entry to the hash bucket at the generated hash value is empty, the supplied output pointer is stored in that address on the second pipeline clock cycle. The (Hariguchi, Col 8, ln. 56 – Col. 9, ln. 7).

The allocating memory blocks to each respective hash table based on the size of the respective hash table is not shown in *Hariguchi*. The Office Action's contention that hash bucket 160 comprises memory blocks for storing route entries; the size of the route entries in the hash bucket of the hash table is "a size of the hash table" is conclusory and goes outside the four corners of the document as *Hariguchi* contains no such teaching. The hash bucket 160 of the *Hariguchi* reference stores network addresses and output pointers at addresses corresponding to the hash value of their associated masked destination addresses. (*Hariguchi*, Column 6, Line 66 to Column 7, Line

2). *Hariguchi* contains no teaching or suggestion of memory blocks or of a mechanism for allocating memory blocks based on a size of the hash table.

Therefore, Claims 1, 5-14 and 18-20 are not anticipated by the *Hariguchi* reference. Accordingly, the Applicants respectfully request withdrawal of the § 102 rejections and full allowance of Claims 1, 5-1 and 18-20 and their dependent claims.

III. CLAIM REJECTIONS -- 35 U.S.C. § 103

Claims 2, 3, 15 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hariguchi reference in view of U.S. Patent Application No. 2001/0027479 to *Delaney, et al.* (hereinafter "Delaney"). The Applicants respectfully traverse the rejection.

Claims 4 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hariguchi reference in view of U.S. Patent No. 6,625,612 to *Tal, et al.* (hereinafter "Tal"). The Applicants respectfully traverse the rejection.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a prima facie case of obviousness. MPEP § 2142, p. 2100-133 (8th ed. rev. 4, October 2005). Absent such a prima facie case, the applicants are under no obligation to produce evidence of nonobviousness. *Id.* To establish a *prima facie* case of obviousness, three basic criteria must be met: *Id.* First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. *Id.* Second, there must be a reasonable expectation of success. *Id.* Finally, the prior art reference (or references when combined) must teach or suggest all the claim

limitations. *Id.* The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicants' disclosure. *Id.*

Claims 2-4 and 22 depend from, and further limit, independent Claim 1. Claims 15-17 depend from, and further limit, independent Claim 14. These claims are allowable for at least the reason as the claims from which they depend, discussed above.

Accordingly, the Applicants respectfully request that the Examiner withdraw the § 103 rejection with respect to these claims.

IV. ALLOWABLE SUBJECT MATTER

The Examiner objected to Claim 21, but suggested that Claim 21 would be allowable if it were rewritten to over come the rejections under 35 U.S.C. 112, second paragraph, set forth in this office action and to include all of the limitations of the base claim and any intervening claims. Applicants thank the Examiner for this suggestion and have amended Claim 21 herein.

CONCLUSION

As a result of the foregoing, the Applicants assert that the remaining Claims in the Application are in condition for allowance, and respectfully request an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at ***ddoyle@munckcarter.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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